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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/636,087	08/06/2003	Thomas C. Savell	6407P239	9834

21186 7590 02/06/2008

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EXAMINER	
SAUNDERS JR, JOSEPH	
ART UNIT	**PAPER NUMBER**
2615	
MAIL DATE	**DELIVERY MODE**
02/06/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/636,087	SAVELL, THOMAS C.	
	Examiner	Art Unit	
	Joseph Saunders	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62 and 64-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-62 and 64-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 17, 2007 has been entered. Claims 1 – 62 and 64 – 71 are currently pending and considered below.

Response to Arguments

2. Applicant's arguments based on the amended claims, see page 17 lines 16 – 20, filed October 17, 2003, with respect to the rejection(s) of claim(s) 1 – 62 and 64 – 71 under 35 U.S.C. 102 and 103 as anticipated by Borland et al. (US 6,724,772) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Naylor (GB 2377138) and also Naylor in view of Edens et al. (US 6,611,537) and Borland et al. (US 6,724,772).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 2, 19 – 21, 24 – 27, 70, and 71 are rejected under 35 U.S.C. 102(a) as being anticipated by Naylor (GB 2377138), hereinafter Naylor.

Claim 1: Naylor discloses a digital processing integrated circuit ("Ring Bus Structure For System on Chip Integrated Circuits") to process media data ("An example of its use in a telecommunications application would be the processing of audio data," page 10 lines 22 – 24), the integrated circuit including: a data path (C1L, C1R, Link In, and Link Out) arranged within the integrated circuit in a ring configuration ("Ring Bus" and Figures 5 – 7); a plurality of processing modules (multiple occurrences of module 1) positioned within the data path to process the media data (module 1 is represented by pipe 9 and unit 11 in Figures 5 – 7); and a digital interface to communication with a device external to the integrated circuit (host peripheral 13), wherein the data path comprises a plurality of separate portions to communicate data between adjacent of the processing modules (CL1, C1R, Link In, and Link Out), wherein the separate portions of the data path couple the adjacent processing modules in series to communicate the media data between the adjacent processing modules ("the bus structure comprises a plurality of interface modules which are connected in series to form the bus structure, where each module is operable to transfer data to at least one adjacent module in the series," Abstract), wherein media data is clocked ("in the synchronous case all actions take place with respect to a clock edge," page 6 lines 35 – 36) between the adjacent

processing modules around the separate portions of the data path to provide communications from a source processing module to a target processing module ("source" and "destination," page 9 line 32 – page 10 line 14), and wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules ("The data packet can be a priority transfer so that the link controller 7 routes the data input directly to the data output of the module," page 4 lines 31 – 34).

Claim 2: Naylor discloses the integrated circuit of claim 1, wherein the data path defines a media data path including a digital audio bus ("An example of its use in a telecommunications application would be the processing of audio data," page 10 lines 22 – 24) that interconnects the plurality of processing modules in series ("the bus structure comprises a plurality of interface modules which are connected in series to form the bus structure, where each module is operable to transfer data to at least one adjacent module in the series," Abstract), and wherein data is communicated around the ring configuration in a single direction on the data path between adjacent processing modules ("The single port module shown in Figures 1 and 2 is a uni-directional device," page 4 lines 35 – 36).

Claim 19: Naylor discloses the integrated circuit of claim 1, wherein the data path includes a transport bus to communicate data between an external memory that is separate from the integrated circuit and at least one of the plurality of processing

modules of the integrated circuit ("Data from an input source can be routed to multiple host peripherals: a DSP for coding and transmission, a voice recognition module for a command interface, and a memory store if a memo function is required, for example," page 10 lines 25 – 29).

Claim 20: Naylor discloses the integrated circuit of claim 1, wherein the plurality of processing modules are digital audio processing modules selected from the group consisting of an audio memory transport module, a digital delay line module, a sample rate converter module, a filter module, a mixer module, a DSP module, and a digital Input/Output module ("Data from an input source can be routed to multiple host peripherals: a DSP for coding and transmission, a voice recognition module for a command interface, and a memory store if a memo function is required, for example," page 10 lines 25 – 29).

Claim 21: Naylor discloses the integrated circuit of claim 1, wherein the integrated circuit is in a very large scale integration (VLSI) device (The integrated circuit is a system on chip and there a VLSI device, Abstract).

Claim 24: Naylor discloses a method to process media data ("An example of its use in a telecommunications application would be the processing of audio data," page 10 lines 22 – 24) in a plurality of processing modules in a digital media processing integrated circuit ("Ring Bus Structure For System on Chip Integrated Circuits"), the method

including: communicating, at each processing module (multiple occurrences of module 1) within the integrated circuit, the media data from the processing module to an adjacent processing module along a data path (CL1, C1R, Link In, and Link Out) interconnecting the plurality of processing modules (module 1 is represented by pipe 9 and unit 11 in Figures 5 – 7) in a ring configuration ("Ring Bus" and Figures 5 – 7) until media data from a source processing module is received at a target processing module of the plurality of processing modules ("When the data packet reaches its destination, the data is read and is not transferred to the next link," page 9 line35 – page 10 line 2); and communicating media data between the data path and a device external to the integrated circuit (host peripheral 13),wherein the processing modules are positioned within the data path and coupled in series ("the bus structure comprises a plurality of interface modules which are connected in series to form the bus structure, where each module is operable to transfer data to at least one adjacent module in the series," Abstract), wherein the media data is clocked ("in the synchronous case all actions take place with respect to a clock edge," page 6 lines 35 – 36) between adjacent processing modules around separate portions of the data path to provide communications from the source processing module to the target processing module ("source" and "destination," page 9 line 32 – page 10 line 14), and wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules ("The data packet can be a priority transfer so that the link controller 7 routes the data input directly to the data output of the module," page 4 lines 31 – 34).

Claim 25: Naylor discloses the method of claim 24, which includes communicating the media data sequentially between the plurality of processing modules ("Data is passed along a series of processes in sequence," page 1 lines 33 – 35).

Claim 26: Naylor discloses the method of claim 24, wherein the data path includes a processing module identifier that identifies the source processing module that provides the media to the data path ("source identifier," page 10 lines 9 – 14).

Claim 27: Naylor discloses the method of claim 24, last processing module of the plurality of processing modules is communicated to first processing module of the plurality of processing modules ("the bus architecture can take the form of a ring when the last link in a chain of links is attached to the first link in the chain; this allows data to be transferred between all links in the chain," page 5 lines 20 – 23).

Claim 70: Naylor discloses the integrated circuit of claim 1, wherein each processing module includes an input to receive data sent by a first adjacent processing module over a first of the separate portions, and an output to send data to a second adjacent processing module over a second of the separate portions to allow serial interconnection of the processing modules in the ring configuration (C1L, C1R, Link In, and Link Out, Figure 1).

Claim 71: Naylor discloses the integrated circuit of claim 70, wherein the input includes at least one input register connected by the data path to the first adjacent processing module (buffer with registers, Figure 1), and the output includes at least one output register connected by the data path to the second adjacent processing module (output multiplexer acts as a register since it is regulated by the link controller) and media data is clocked along the data path by the at least one input register and the at least one output register (page 6 lines 25 – 36).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 – 18, 22, 23, 28 – 62, and 64 – 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naylor in view of Edens et al. (US 6,611,537 B1), hereinafter Edens, and Borland et al. (US 6,724,772 B1), hereinafter Borland.

Claims 3 – 18: Naylor discloses the integrated circuit of claims 1 – 2, and while Naylor discloses synchronous operation based on a clock edge, Naylor does not disclose the use of a multiplexing scheme such as time division multiplexing and also does not disclose the use of a control data path to communicate processing control data and therefore does not disclose the limitation presented in claims 3 – 18. Naylor also

discloses a disadvantage of the architecture in that since the sequence of transfers are treated as continuous, no host peripheral between source and destination is allowed to insert a package midway through the sequence, thereby resulting in delay (page 7 lines 16 – 27). Edens gives a general teaching of processing digital media streams in a ring configuration (Figure 7) similar to Naylor's configuration and teaches in column 8 under "4. Synchronous Networks and Ring Networks" (see also column 25, "2. Synchronous Logical Ring Network Architecture") that it is possible to enable more than one device to insert information by using "time slices", effectively eliminating delay as disclosed by Naylor. Borland also discloses the use of TDMA in a ring configuration for audio processing and gives further information on how to implement such a system. During the implementation disclosed by Borland other advantageous features are realized by including a control data path and an arbitration technique that for example allows for the adjustment of data rate of individual channels.

Regarding Claim 3, Borland discloses wherein the digital audio bus communicates digital audio data in a plurality of time-slots ("The bus controller 350 may enable data transfers on the TDMA bus 330 only during assigned time slots of assigned frequency and assigned length," Column 5 Lines 55 – 59), each particular processing module having at least one programmable or fixed time-slot from which data is received from the data path for processing by the particular processing module ("The schedule includes information on time slot assignments for one or more of the plurality of modules," Column 6 Lines 6 – 11) and wherein media data corresponding to different processing modules is present at the same time on the data path (Since this is TDMA

system media data corresponding to different processing modules is present in different time slots or "at the same time" referring to absolute time, on the data path, Column 5 Lines 55 – 59).

Regarding Claim 4, Borland discloses wherein the digital audio bus communicates digital audio data in a plurality of time-slots, each particular processing module being assigned at least one time-slot into which data processed by the particular processing module is exported to the digital audio bus ("If the timing indicates real-time or fast response, then the bus controller 350 may assign multiple contiguous time slots to the data transfer associated with that request. Time slots may be set with any frequency and/or length, as desired," Column 6 Lines 1 – 5) and wherein media data corresponding to different processing modules is present at the same time on the data path (Since this is TDMA system media data corresponding to different processing modules is present in different time slots or "at the same time" referring to absolute time, on the data path, Column 5 Lines 55 – 59).

Regarding Claim 5, Borland discloses wherein one of the processing modules is a Digital Signal Processor (DSP) (bus controller 350) and the data path communicates processing control data in a plurality of time-slots that are allocated to the processing modules under control of the DSP ("the bus controller 350 includes, or has direct access to, a memory 315, which stores a schedule of the data transfers." "The bus controller examines the schedule when a new request is received and allocated unused time slots for the new request," Column 6 Lines 6 – 24).

Regarding Claim 6, Borland discloses the data path comprise time division multiplexed buses ("bus 330 is a time division, multiple access (TDMA) bus", Column 5 Lines 55 – 59) to communicate a plurality of audio channels (audio data in different time slots).

Regarding Claim 7, Borland discloses wherein the data path communicates data between the plurality of processing modules at bit rates that differ ("If the timing indicates real-time or fast response, then the bus controller 350 may assign multiple contiguous time slots to the data transfer associated with that request. Time slots may be set with any frequency and/or length, as desired," Column 6 Lines 1 – 5).

Regarding Claim 8, Borland discloses wherein the media data path includes a total number of time-slots for communicating media data at a plurality of different bit rates, and wherein the sum of a number of time-slots allocated to each one of the plurality of bit rates equals the total number of time-slots summed across every bit rate ("If the timing indicates real-time or fast response, then the bus controller 350 may assign multiple contiguous time slots to the data transfer associated with that request. Time slots may be set with any frequency and/or length, as desired," Column 6 Lines 1 – 5. Therefore, the sum of a number of time-slots allocated to each one of the plurality of bit rates equals the total number of time-slots summed across every bit rate).

Regarding Claim 9, Borland discloses wherein each processing module is configured to: selectively extract media data for processing from the data path, the media data being provided in at least one time-slot (TDMA, Column 5 Lines 55 – 59) of the data path allocated to the processing module; selectively insert processed media

data into its allocated time-slot; and pass media data that it receives and that is associated with other processing modules unchanged along the data path (Data is passed from module to module in a manner controlled by the bus controller and task specific or task general processing takes place at each module, Column 4 Lines 1 – 5, Column 6 Lines 24 – 35).

Regarding Claim 10, Borland discloses the integrated circuit of claim 1, wherein the number of processing modules connected along the data path is configurable, each processing module included in the device being allocated at least one time-slot provided by the data path (Borland discloses that the integrated circuit 100 contains "a plurality of modules 210," Column 5 Lines 14 – 19, and therefore allows for the number of modules to be configurable).

Regarding Claim 11, Borland discloses wherein the data path includes a control data path ("integrated circuit 100 includes a unified data, address, and control bus 330, or a separate data bus 330 and control bus 332," Column 6 Lines 24 – 36) to communicate processing control data (transfer requests) to at least one processing module, the processing control data being used by the processing module to process digital data received from the data path (Transfer requests provide identifier information, transfer size, and timing information necessary for the processing module to process the digital data received from the data path, Column 5 Lines 24 – 36).

Regarding Claim 12, Borland discloses wherein the processing control data includes parameters for digital signal processing by the processing module (Transfer requests provide identifier information, transfer size, and timing information necessary

for the processing module to process the digital data received from the data path, Column 5 Lines 24 – 36).

Regarding Claim 13, Borland discloses wherein the parameters include at least one of filter parameters, time delay parameters ("The bus controller examines the priority value and the timing value when the bus controller analyzes the request for transfer," enabling for example previously scheduled requests to be reassigned or delayed to later time slots, as necessary, Column 6 Lines 6 – 23. This information is provided in the transfer requests or control data.), mixing parameters, or sample-rate conversion parameters.

Regarding Claim 14, Borland discloses wherein the control data path ("integrated circuit 100 includes a unified data, address, and control bus 330, or a separate data bus 330 and control bus 332," Column 6 Lines 24 – 36) is a time division multiplexed bus arranged to interconnect the plurality of modules in the ring configuration (Figures 2 and 3) and wherein while the media data is communicated from the source processing module to the target processing module, any one or more of the processing modules can add media data to or receive media data from the media data path (Since the modules are serially connected the modules and the bus is a TDMA bus, data is passed through all modules starting with the source however is only processed at the appropriate destination module, Column 1 Line 39 – Column 2 Line 44 and Column 5 Lines 55 – 59).

Regarding Claim 15, Borland discloses wherein the processing control data includes streams of processing control data each of which is associated with a stream

of media data communicated via the data path, each stream of processing control data being destined for an associated target processing module to which the stream of media data is communicated ("Streams" of data are communicated in time slots on buses 330 and 332 and the buses may be serial or parallel, the control data is associated with the media data and tells the associated target processing module how to process the media data, Column 1 Line 39 – Column 2 Line 44).

Regarding Claim 16, Borland discloses wherein each stream of processing control data is arranged to be communicated via the control data path to arrive at its associated target processing module prior to a source processing module exporting the media data to the media data path ("bus controller examines the priority value and the timing value when the bus controller analyzes the request for the transfer," Column 6 Lines 21 – 23).

Regarding Claim 17, Borland discloses wherein the data path includes: a plurality of media channels (time slots for audio data) defined by time division multiplexed time-slots; and a channel identification path (address bus) including channel identification data ("an identifier which identifies one or more receiving modules 210," Column 5 Lines 24 – 29) to identify each media channel to the plurality of processing modules (Column 6 Lines 24 – 26).

Regarding Claim 18, Borland discloses wherein the data path includes a control data path (control bus) to communicate processing control data to at least one processing module (modules 210), the control data path including a plurality of control channels (time slots) defined by time division multiplexed time-slots, wherein the

channel identification path identifies both the media channels and the control channels (address bus includes identification information of the individual time slots corresponding to both the control and data buses) (Column 6 Lines 24 – 36).

Therefore, given the teachings of Edens and Borland it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate TDMA and associated features in the system of Naylor, thereby improving the performance of the system of Naylor by eliminating the aforementioned disadvantages.

Claims 28 – 35: Claims 28 – 35 are substantially similar in scope to claims 3 – 8 and 11 and therefore are rejected for the same reasons.

Claims 36 – 46: Claims 36 – 46 are substantially similar in scope to claims 10 – 20 and therefore are rejected for the same reasons.

Claims 47 – 62 and 64 – 69: Claims 47 – 62 and 64 – 69 are substantially similar in scope to claims 24 – 46 and therefore are rejected for the same reasons.

Claim 22: Naylor discloses a digital processing integrated circuit ("Ring Bus Structure For System on Chip Integrated Circuits") to process media data ("An example of its use in a telecommunications application would be the processing of audio data," page 10 lines 22 – 24), the integrated circuit including: a media data path (C1L, C1R, Link In, and Link Out) arranged within the integrated circuit in a ring configuration ("Ring Bus"

and Figures 5 – 7); a plurality of processing modules (multiple occurrences of module1) positioned within the media data path and coupled in series to process the media data ("the bus structure comprises a plurality of interface modules which are connected in series to form the bus structure, where each module is operable to transfer data to at least one adjacent module in the series," Abstract); a digital interface to communicate media data with a device external to the integrated circuit (host peripheral 13), wherein the media data is clocked between adjacent processing modules around separate portions of the data path ("in the synchronous case all actions take place with respect to a clock edge," page 6 lines 35 – 36) to provide communications from the source processing module to the target processing module ("source" and "destination," page 9 line 32 – page 10 line 14), and wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules ("The data packet can be a priority transfer so that the link controller 7 routes the data input directly to the data output of the module," page 4 lines 31 – 34).

Naylor does not disclose the integrated circuit including a processing control data path to communicate processing control data between the adjacent processing modules, wherein the processing control data defines processing functionality at an associated processing module and wherein each processing module of the plurality of processing modules is configured to communicate the media data and the processing control data to an adjacent processing module; and a routing controller to route the

media data and the processing control data along the data path to an associated processing module.

Naylor also discloses a disadvantage of the architecture in that since the sequence of transfers are treated as continuous, no host peripheral between source and destination is allowed to insert a package midway through the sequence, thereby resulting in delay (page 7 lines 16 – 27). Edens gives a general teaching of processing digital media streams in a ring configuration (Figure 7) similar to Naylor's configuration and teaches in column 8 under "4. Synchronous Networks and Ring Networks" (see also column 25, "2. Synchronous Logical Ring Network Architecture") that it is possible to enable more than one device to insert information by using "time slices", effectively eliminating delay as disclosed by Naylor. Borland also discloses the use of TDMA in a ring configuration for audio processing and gives further information on how to implement such a system. During the implementation disclosed by Borland other advantageous features are realized by including a control data path and an arbitration technique that for example allows for the adjustment of data rate of individual channels.

Borland goes on to teach a processing control data path to communicate processing control data between the adjacent processing modules (two circular buses, 330 and 332), wherein the processing control data (transfer requests) defines processing functionality at an associated processing module (Transfer requests provide identifier information, transfer size, and timing information necessary for the processing module to process the digital data received from the data path, Column 5 Lines 24 – 36.) and wherein each processing module of the plurality of processing modules is

configured to communicate the media data and the processing control data to an adjacent processing module (Since processing modules are arranged in a ring configuration the data must be passed to an adjacent processing module). Finally, Borland discloses the integrated circuit including a routing controller (bus controller 350) to route the media data and the processing control data along the data path to an associated processing module. The bus controller provides the advantage of assigning multiple contiguous time slots to the data transfer associated with a request allowing for real-time or fast response (Column 6 Lines 1 – 5).

Therefore, given the teachings of Edens and Borland it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a control data path defining processing functionality along with a routing controller and the associated TDMA feature in the system of Naylor, thereby improving the performance of the system of Naylor by eliminating the aforementioned disadvantages.

Claim 23: Naylor, Edens, and Borland disclose the integrated circuit of claim 22, and Naylor further discloses wherein while the media data is communicated from the source processing module to the target processing module, any one or more of the processing modules can add media data to or receive media data from the media data path ("each module is operable to transfer data to at least one adjacent module in the series," Abstract).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Saunders whose telephone number is (571) 270-1063. The examiner can normally be reached on Monday - Thursday, 9:00 a.m. - 4:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
January 28, 2008

SINH TRAN
SUPERVISORY PATENT EXAMINER